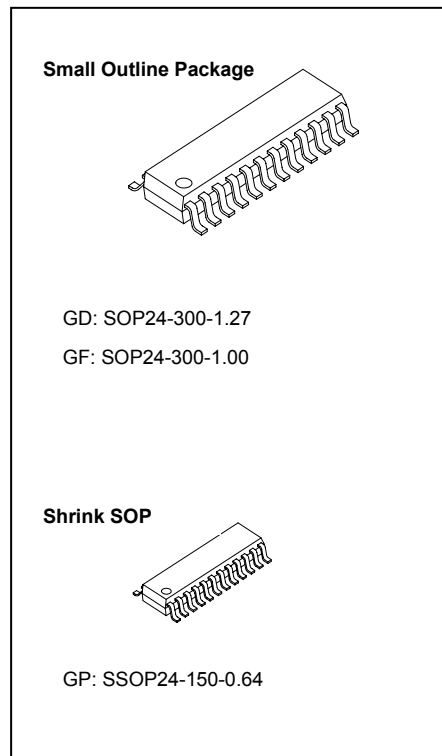




16-channel Constant Current LED Sink Driver

Features

- 16 constant-current output channels
- Constant output current invariant to load voltage change:
Constant output current range:
3 - 45 mA @ $V_{DD} = 5V$;
3 - 30 mA @ $V_{DD} = 3.3V$
- Excellent output current accuracy:
between channels: $\pm 3\%$ (max.), and
between ICs: $\pm 6\%$ (max.)
- Output current adjusted through an external resistor
- Fast response of output current, \overline{OE} (min.): 250 ns @ $V_{DD} = 5.0V$
- Staggered output delay
- 25MHz clock frequency
- Schmitt trigger input
- 3.3V/ 5V supply voltage
- "Pb-free & Green" Package



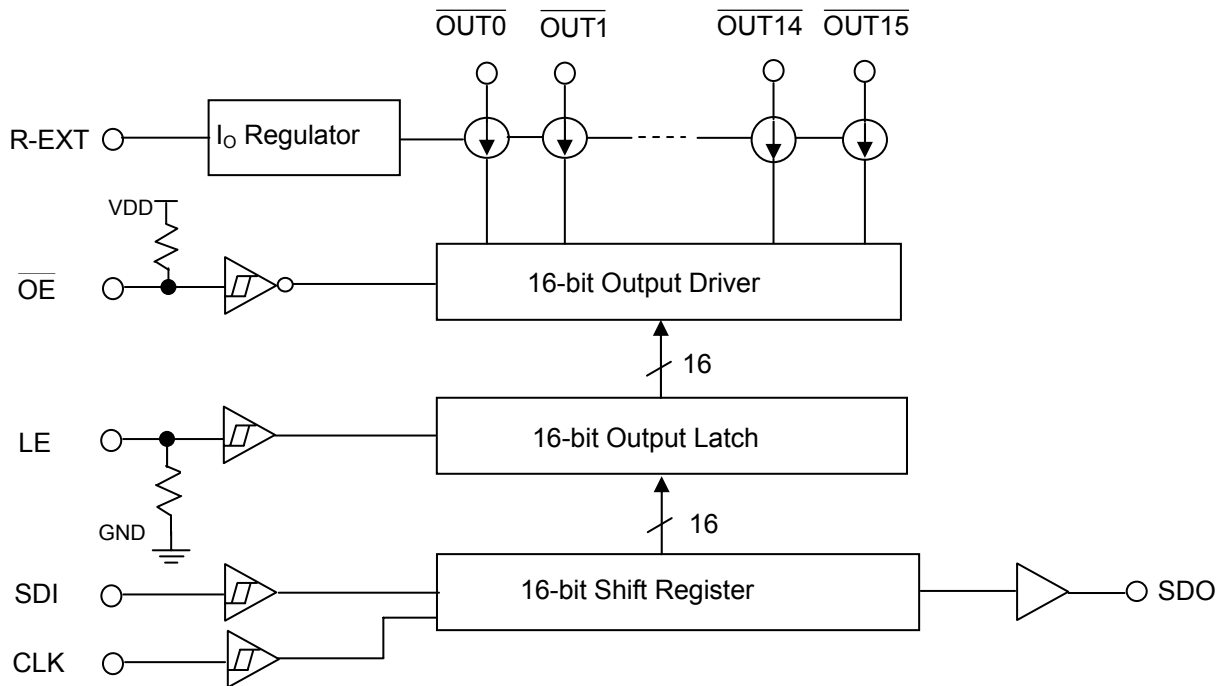
| Current Accuracy | | Conditions |
|------------------|-------------|--|
| Between Channels | Between ICs | |
| < $\pm 3\%$ | < $\pm 6\%$ | $I_{OUT} = 3 \text{ mA} \sim 30 \text{ mA} @ V_{DS} = 0.8V ; V_{DD} = 3.3V$ $I_{OUT} = 3 \text{ mA} \sim 45 \text{ mA} @ V_{DS} = 0.8V ; V_{DD} = 5.0V$ |

Product Description

With PrecisionDrive™ technology, MBI5025 is designed for LED displays which require to operate at low current and to match the luminous intensity of each channel. It provides supply voltage and accepts CMOS logic input at 3.3V and 5.0V to meet the trend of low power consumption. MBI5025 contains a serial buffer and data latches which convert serial input data into parallel output format. At MBI5025 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of V_F variations.

MBI5025 provides users with great flexibility and device performance while using MBI5025 in their system design for LED display applications, e.g. LED panels. It accepts an input voltage range from 3V to 5.5V and maintains a constant current up from 3 mA to 45 mA determined by an external resistor, R_{ext} , which gives users flexibility in controlling the light intensity of LEDs. MBI5025 guarantees to endure maximum 17V at the output port. The high clock frequency, 25 MHz, also satisfies the system requirements of high volume data transmission.

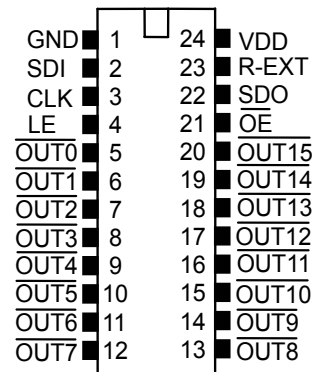
Block Diagram



Terminal Description

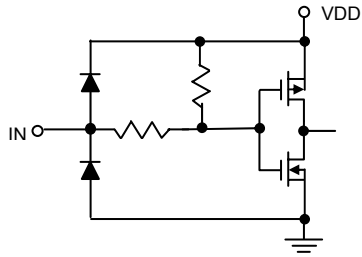
| Pin No. | Pin Name | Function |
|---------|---|--|
| 1 | GND | Ground terminal for control logic and current sink |
| 2 | SDI | Serial-data input to the shift register |
| 3 | CLK | Clock input terminal for data shift on rising edge |
| 4 | LE | Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low. |
| 5~20 | $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ | Constant current output terminals |
| 21 | $\overline{\text{OE}}$ | Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked). |
| 22 | SDO | Serial-data output to the following SDI of next driver IC. SDO signal change on rising edge of CLK. |
| 23 | R-EXT | Input terminal used to connect an external resistor for setting up output current for all output channels |
| 24 | VDD | 3.3V / 5V supply voltage terminal |

Pin Configuration

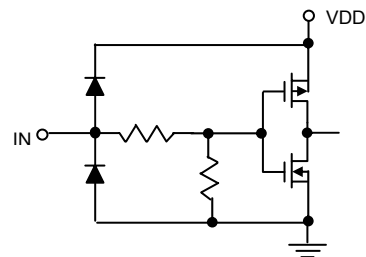


Equivalent Circuits of Inputs and Outputs

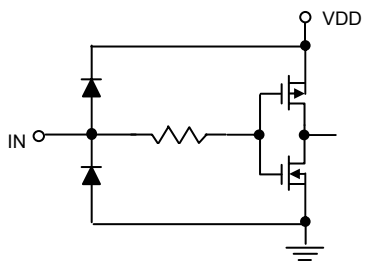
\overline{OE} terminal



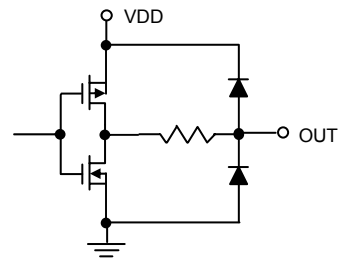
LE terminal



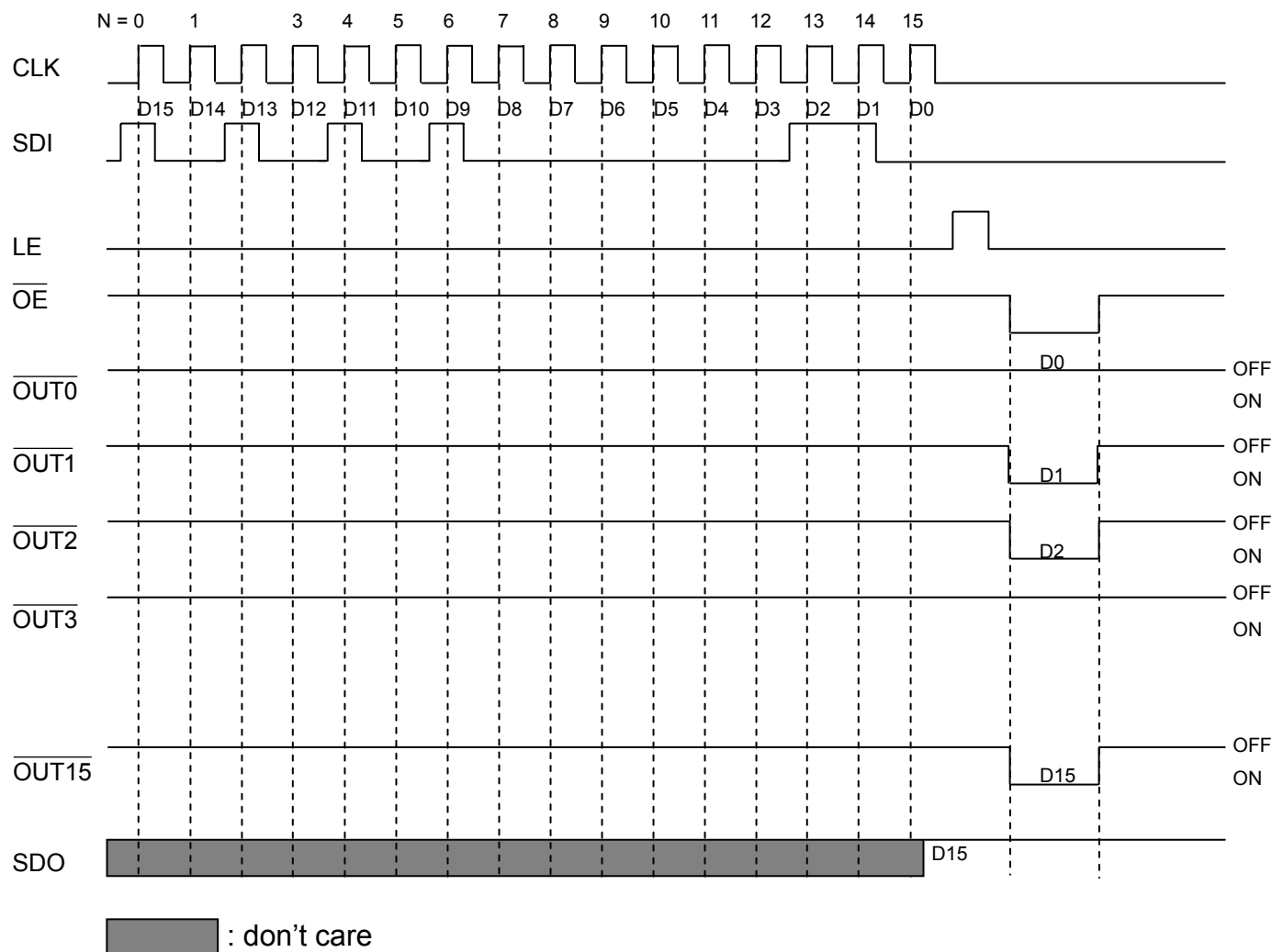
CLK, SDI terminal



SDO terminal



Timing Diagram



Truth Table

| CLK | LE | OE | SDI | $\overline{OUT0} \dots \overline{OUT7} \dots \overline{OUT15}$ | SDO |
|-----|----|----|------------------|---|-------------------|
| | H | L | D _n | $\overline{D_n} \dots \overline{D_{n-7}} \dots \overline{D_{n-15}}$ | D _{n-15} |
| | L | L | D _{n+1} | No Change | D _{n-14} |
| | H | L | D _{n+2} | $\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$ | D _{n-13} |
| | X | L | D _{n+3} | $\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$ | D _{n-13} |
| | X | H | D _{n+4} | Off | D _{n-13} |

Maximum Ratings

| Characteristic | | Symbol | Rating | Unit |
|---|-----------|---------------|-----------------------|--------------------|
| Supply Voltage | | V_{DD} | 0 ~ 7.0 | V |
| Input Voltage | | V_{IN} | -0.4 ~ $V_{DD} + 0.4$ | V |
| Output Current | | I_{OUT} | +90 | mA |
| Sustaining Voltage at OUT Port | | V_{DS} | -0.5 ~ +17.0 | V |
| Clock Frequency | | F_{CLK} | 25 | MHz |
| GND Terminal Current | | I_{GND} | +1000 | mA |
| Power Dissipation (On PCB, $T_a=25^\circ\text{C}$) | GD– type | P_D | 2.88 | W |
| | GF – type | | 1.88 | |
| | GP – type | | 1.76 | |
| Thermal Resistance (On PCB, $T_a=25^\circ\text{C}$) | GD– type | $R_{th(j-a)}$ | 46.60 | $^\circ\text{C/W}$ |
| | GF – type | | 66.66 | |
| | GP – type | | 70.90 | |
| Operating Temperature | | T_{opr} | -40 ~ +85 | $^\circ\text{C}$ |
| Storage Temperature | | T_{stg} | -55 ~ +150 | $^\circ\text{C}$ |

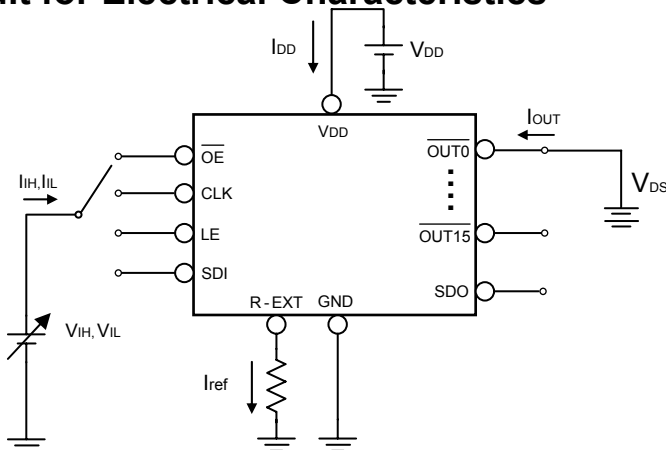
Electrical Characteristics (V_{DD} = 5.0V)

| Characteristics | | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|--|-----------|------------------------|--|--------------------------|---------------------|------|---------------------|-------|
| Supply Voltage | | V _{DD} | - | | 4.5 | 5.0 | 5.5 | V |
| Sustaining Voltage at OUT Ports | | V _{DS} | $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ | | - | - | 17.0 | V |
| Output Current | | I _{OUT} | Refer to "Test Circuit for Electrical Characteristics" | | 3 | - | 45 | mA |
| | | I _{OH} | SDO | | - | - | -1.0 | mA |
| | | I _{OL} | SDO | | - | - | 1.0 | mA |
| Input Voltage | "H" level | V _{IH} | Ta = -40~85°C | | 0.7*V _{DD} | - | V _{DD} | V |
| | "L" level | V _{IL} | Ta = -40~85°C | | GND | - | 0.3*V _{DD} | V |
| Output Leakage Current | | I _{OH} | V _{DS} = 17.0V | | - | - | 0.5 | μA |
| Output Voltage | SDO | V _{OL} | I _{OL} = +1.0mA | | - | - | 0.4 | V |
| | | V _{OH} | I _{OH} = -1.0mA | | 4.6 | - | - | V |
| Output Current 1 | | I _{OUT1} | V _{DS} = 1.0V | R _{ext} = 1860Ω | - | 10 | - | mA |
| Current Skew | | dI _{OUT1} | I _{OL} = 10mA V _{DS} = 1.0V | R _{ext} = 1860Ω | - | ±1 | ±3 | % |
| Output Current 2 | | I _{OUT2} | V _{DS} = 1.0V | R _{ext} = 744Ω | - | 25 | - | mA |
| Current Skew | | dI _{OUT2} | I _{OL} = 25mA V _{DS} = 1.0V | R _{ext} = 744Ω | - | ±1 | ±3 | % |
| Output Current vs. Output Voltage Regulation | | %/dV _{DS} | V _{DS} within 1.0V and 3.0V | | - | ±0.1 | - | % / V |
| Output Current vs. Supply Voltage Regulation | | %/dV _{DD} | V _{DD} within 4.5V and 5.5V | | - | ±1.0 | - | % / V |
| Pull-up Resistor | | R _{IN(up)} | $\overline{\text{OE}}$ | | 250 | 500 | 800 | KΩ |
| Pull-down Resistor | | R _{IN(down)} | LE | | 250 | 500 | 800 | KΩ |
| Supply Current | "OFF" | I _{DD(off) 1} | R _{ext} = Open, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}} = \text{Off}$ | | - | 2.4 | 5.0 | mA |
| | | I _{DD(off) 2} | R _{ext} = 1860Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}} = \text{Off}$ | | - | 4.3 | 7.0 | |
| | | I _{DD(off) 3} | R _{ext} = 744Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}} = \text{Off}$ | | - | 5.7 | 9.0 | |
| | "ON" | I _{DD(on) 1} | R _{ext} = 1860Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}} = \text{On}$ | | - | 4.6 | 8.5 | |
| | | I _{DD(on) 2} | R _{ext} = 744Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}} = \text{On}$ | | - | 6.0 | 9.5 | |

Electrical Characteristics (V_{DD} = 3.3V)

| Characteristics | | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|-----------|------------------------|---|---------------------|------|---------------------|-------|
| Supply Voltage | | V _{DD} | - | 3.0 | 3.3 | 4.5 | V |
| Sustaining Voltage at OUT Ports | | V _{DS} | $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ | - | - | 17.0 | V |
| Output Current | | I _{OUT} | Refer to "Test Circuit for Electrical Characteristics" | 3 | - | 30 | mA |
| | | I _{OH} | SDO | - | - | -1.0 | mA |
| | | I _{OL} | SDO | - | - | 1.0 | mA |
| Input Voltage | "H" level | V _{IH} | Ta = -40~85°C | 0.7*V _{DD} | - | V _{DD} | V |
| | "L" level | V _{IL} | Ta = -40~85°C | GND | - | 0.3*V _{DD} | V |
| Output Leakage Current | | I _{OH} | V _{DS} = 17.0V | - | - | 0.5 | μA |
| Output Voltage | SDO | V _{OL} | I _{OL} = +1.0mA | - | - | 0.4 | V |
| | | V _{OH} | I _{OH} = -1.0mA | 2.9 | - | - | V |
| Output Current 1 | | I _{OUT1} | V _{DS} = 1.0V R _{ext} = 6200Ω | - | 3 | - | mA |
| Current Skew | | dI _{OUT1} | I _{OL} = 3mA V _{DS} = 1.0V R _{ext} = 6200Ω | - | ±1 | ±3 | % |
| Output Current 2 | | I _{OUT2} | V _{DS} = 1.0V R _{ext} = 744Ω | - | 25 | - | mA |
| Current Skew | | dI _{OUT2} | I _{OL} = 25mA V _{DS} = 1.0V R _{ext} = 744Ω | - | ±1 | ±3 | % |
| Output Current vs. Output Voltage Regulation | | %/dV _{DS} | V _{DS} within 1.0V and 3.0V | - | ±0.1 | - | % / V |
| Output Current vs. Supply Voltage Regulation | | %/dV _{DD} | V _{DD} within 3.0V and 4.5V | - | ±1 | - | % / V |
| Pull-up Resistor | | R _{IN(up)} | $\overline{\text{OE}}$ | 250 | 500 | 800 | KΩ |
| Pull-down Resistor | | R _{IN(down)} | LE | 250 | 500 | 800 | KΩ |
| Supply Current | "OFF" | I _{DD(off) 1} | R _{ext} = Open, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ = Off | - | 1.8 | 5.0 | mA |
| | | I _{DD(off) 2} | R _{ext} = 6200Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ = Off | - | 4.0 | 7.0 | |
| | | I _{DD(off) 3} | R _{ext} = 744Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ = Off | - | 5.2 | 8.5 | |
| | "ON" | I _{DD(on) 1} | R _{ext} = 6200Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ = On | - | 4.5 | 7.0 | |
| | | I _{DD(on) 2} | R _{ext} = 744Ω, $\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$ = On | - | 5.5 | 8.5 | |

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD} = 5.0V)

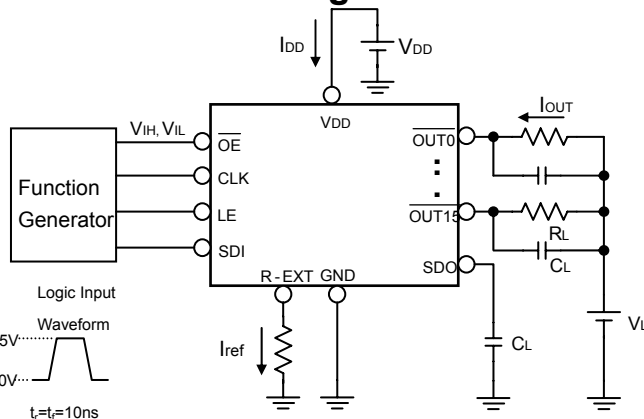
| Characteristics | | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------------|--|---------------------|--|------|------|------|------|
| Propagation Delay Time ("L" to "H") | CLK - $\overline{\text{OUT2n}}$ | t_{pLH1} | V _{DD} =5.0 V V _{DS} =1.0 V V _{IH} =V _{DD} V _{IL} =GND R _{ext} =930 Ω V _L =4.5 V R _L =162 Ω C _L =10 pF | - | 115 | 135 | ns |
| | CLK - $\overline{\text{OUT2n+1}}$ | | | - | 80 | 100 | ns |
| | LE - $\overline{\text{OUT2n}}$ | t_{pLH2} | | - | 115 | 135 | ns |
| | LE - $\overline{\text{OUT2n+1}}$ | | | - | 80 | 100 | ns |
| | $\overline{\text{OE}}$ - $\overline{\text{OUT2n}}$ | t_{pLH3} | | - | 115 | 135 | ns |
| | $\overline{\text{OE}}$ - $\overline{\text{OUT2n+1}}$ | | | - | 80 | 100 | |
| | CLK - SDO | t_{pLH4} | | - | 20 | 40 | ns |
| Propagation Delay Time ("H" to "L") | CLK - $\overline{\text{OUT2n}}$ | t_{pHL1} | | - | 115 | 135 | ns |
| | CLK - $\overline{\text{OUT2n+1}}$ | | | - | 80 | 100 | ns |
| | LE - $\overline{\text{OUT2n}}$ | t_{pHL2} | | - | 115 | 135 | ns |
| | LE - $\overline{\text{OUT2n+1}}$ | | | - | 80 | 100 | ns |
| | $\overline{\text{OE}}$ - $\overline{\text{OUT2n}}$ | t_{pHL3} | | - | 115 | 135 | ns |
| | $\overline{\text{OE}}$ - $\overline{\text{OUT2n+1}}$ | | | - | 80 | 100 | |
| | CLK - SDO | t_{pHL4} | | - | 20 | 40 | ns |
| Pulse Width | CLK | $t_{w(\text{CLK})}$ | 20 | - | - | ns | |
| | LE | $t_{w(\text{L})}$ | 20 | - | - | ns | |
| | $\overline{\text{OE}}$ | $t_{w(\text{OE})}$ | 250 | - | - | ns | |
| Hold Time for LE | | $t_{h(\text{L})}$ | 30 | - | - | ns | |
| Setup Time for LE | | $t_{su(\text{L})}$ | 5 | - | - | ns | |
| Hold Time for SDI | | $t_{h(\text{D})}$ | 5 | - | - | ns | |
| Setup Time for SDI | | $t_{su(\text{D})}$ | 3 | - | - | ns | |
| Maximum CLK Rise Time | | t_r | - | - | 500 | ns | |
| Maximum CLK Fall Time | | t_f | - | - | 500 | ns | |
| SDO Rise Time | | $t_{r,\text{SDO}}$ | - | 10 | - | ns | |
| SDO Fall Time | | $t_{f,\text{SDO}}$ | - | 10 | - | ns | |
| Output Rise Time of Output Ports | | t_{or} | - | 160 | 180 | ns | |
| Output Fall Time of Output Ports | | t_{of} | - | 70 | 90 | ns | |

* Among output channels exist 35ns delay time between odd number $\overline{\text{OUT2n+1}}$ (e.g.:Bit1/Bit3/Bit5...)and even number $\overline{\text{OUT2n}}$ (ex: Bit0/Bit2/Bit4...). MBI5025 has a built-in staggered circuit to perform delay mechanism, by which the even and odd output ports will be turned on at a different time so that the instant current from the power line will be lowered.

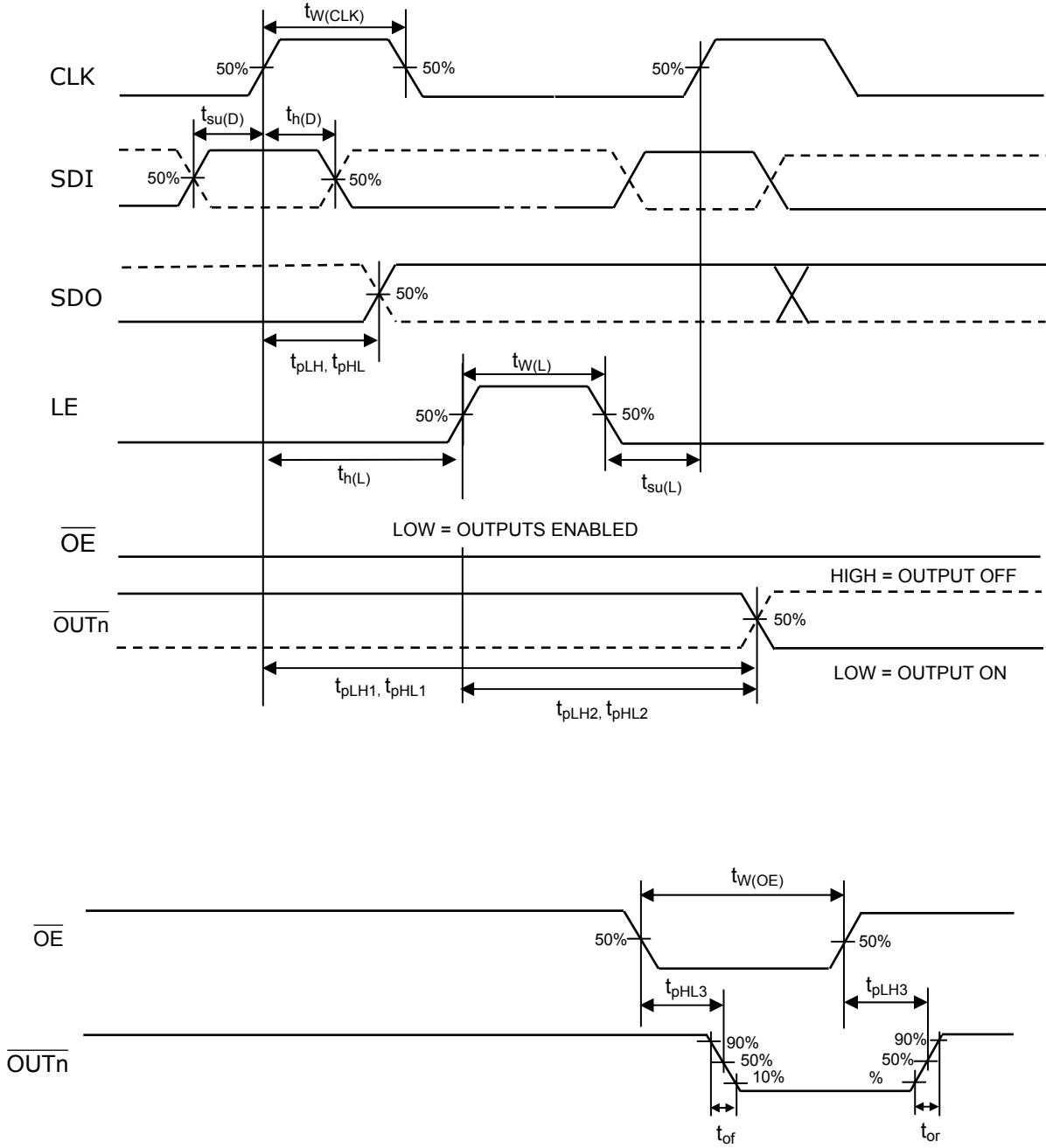
Switching Characteristics ($V_{DD} = 3.3V$)

| Characteristics | | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------------|--|-------------|---|------|------|------|------|
| Propagation Delay Time ("L" to "H") | CLK - $\overline{OUT2n}$ | t_{pLH1} | $V_{DD}=3.3 V$ $V_{DS}=1.0 V$ $V_{IH}=V_{DD}$ $V_{IL}=GND$ $R_{ext}=930 \Omega$ $V_L=4.5 V$ $R_L=162 \Omega$ $C_L=10 pF$ | - | 115 | 135 | ns |
| | CLK - $\overline{OUT2n+1}$ | | | - | 80 | 100 | ns |
| | LE - $\overline{OUT2n}$ | t_{pLH2} | | - | 115 | 135 | ns |
| | LE - $\overline{OUT2n+1}$ | | | - | 80 | 100 | ns |
| | \overline{OE} - $\overline{OUT2n}$ | t_{pLH3} | | - | 115 | 135 | ns |
| | \overline{OE} - $\overline{OUT2n+1}$ | | | - | 80 | 100 | |
| | CLK - SDO | t_{pLH4} | | - | 20 | 40 | ns |
| Propagation Delay Time ("H" to "L") | CLK - $\overline{OUT2n}$ | t_{pHL1} | | - | 115 | 135 | ns |
| | CLK - $\overline{OUT2n+1}$ | | | - | 80 | 100 | ns |
| | LE - $\overline{OUT2n}$ | t_{pHL2} | | - | 115 | 135 | ns |
| | LE - $\overline{OUT2n+1}$ | | | - | 80 | 100 | ns |
| | \overline{OE} - $\overline{OUT2n}$ | t_{pHL3} | | - | 115 | 135 | ns |
| | \overline{OE} - $\overline{OUT2n+1}$ | | | - | 80 | 100 | |
| | CLK - SDO | t_{pHL4} | | - | 20 | 40 | ns |
| Pulse Width | CLK | $t_w(CLK)$ | 20 | - | - | ns | |
| | LE | $t_w(L)$ | 20 | - | - | ns | |
| | \overline{OE} | $t_w(OE)$ | 300 | - | - | ns | |
| Hold Time for LE | | $t_h(L)$ | 30 | - | - | ns | |
| Setup Time for LE | | $t_{su}(L)$ | 5 | - | - | ns | |
| Hold Time for SDI | | $t_h(D)$ | 5 | - | - | ns | |
| Setup Time for SDI | | $t_{su}(D)$ | 3 | - | - | ns | |
| Maximum CLK Rise Time | | t_r | - | - | 500 | ns | |
| Maximum CLK Fall Time | | t_f | - | - | 500 | ns | |
| SDO Rise Time | | $t_{r,SDO}$ | - | 10 | - | ns | |
| SDO Fall Time | | $t_{f,SDO}$ | - | 10 | - | ns | |
| Output Rise Time of Output Ports | | t_{or} | - | 160 | 180 | ns | |
| Output Fall Time of Output Ports | | t_{of} | - | 70 | 90 | ns | |

Test Circuit for Switching Characteristics



Timing Waveform

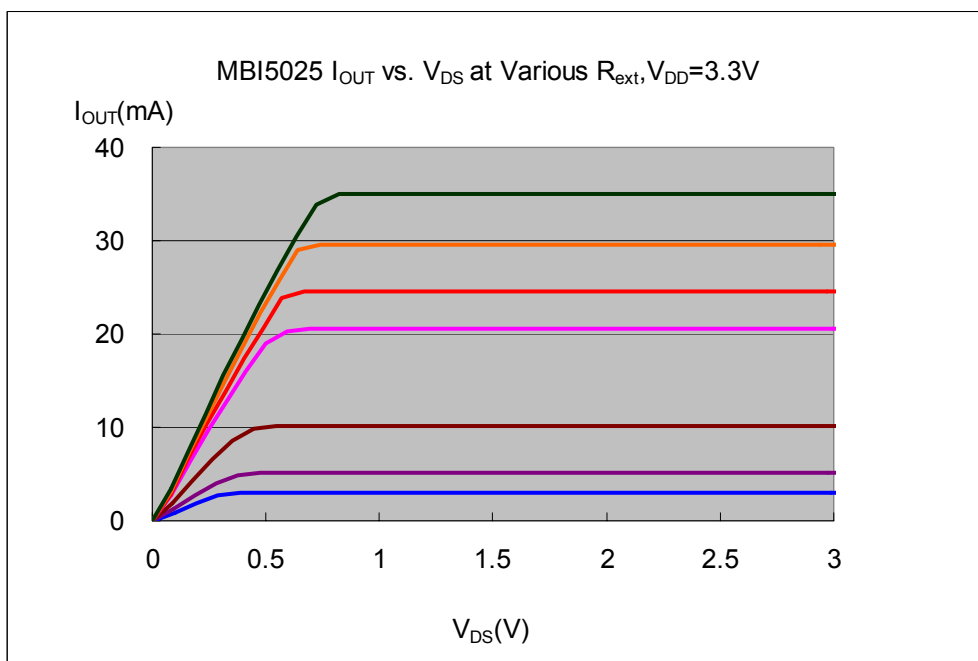
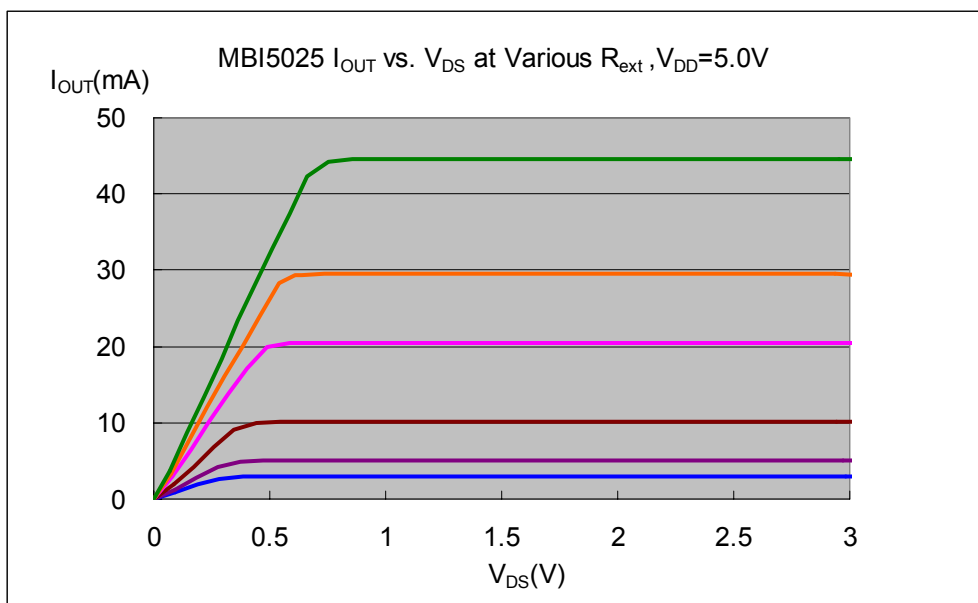


Application Information

Constant Current

To design LED displays, MBI5025 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

- 1) The maximum current variation between channels is less than $\pm 3\%$, and that between ICs is less than $\pm 6\%$.
- 2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This performs as a perfection of load regulation.

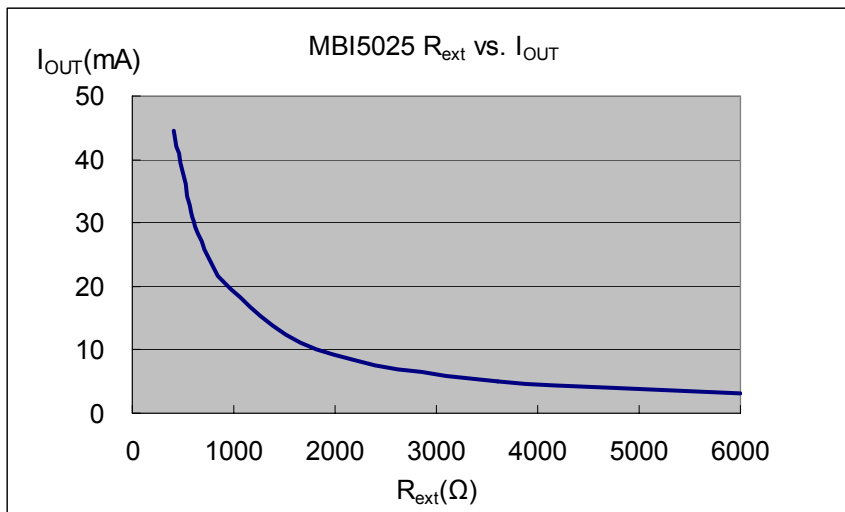


Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{EXT} . The relationship between I_{OUT} and R_{EXT} is shown in the following figure.

Also, the output current can be calculated from the equation:

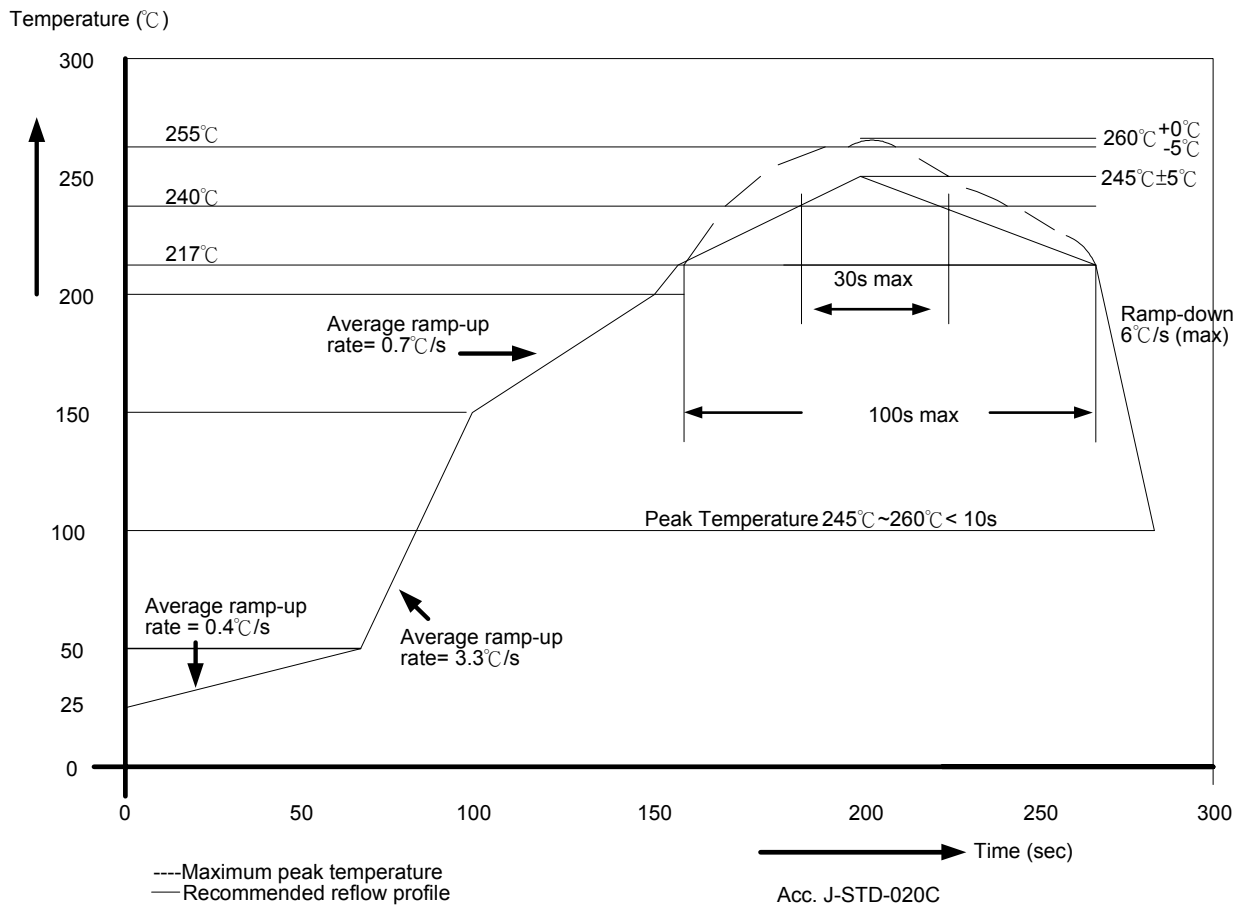
$$V_{R-EXT} = 1.24V ; I_{OUT} = V_{R-EXT} * (1/R_{EXT}) * 15 ; R_{EXT} = (V_{R-EXT} / I_{OUT}) * 15$$



Where R_{EXT} is the resistance of the external resistor connected to R-EXT terminal and V_{R-EXT} is the voltage of R-EXT terminal. The magnitude of current (as a function of R_{EXT}) is around 25mA at 744Ω and 10mA at 1860Ω.

Soldering Process of “Pb-free & Green” Package*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected **100% pure tin (Sn)** to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to standard 215°C to 240°C reflow processes which adopt tin/lead (SnPb) solder paste. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn), will all require up to 260°C for proper soldering on boards, referring to J-STD-020C as shown below.

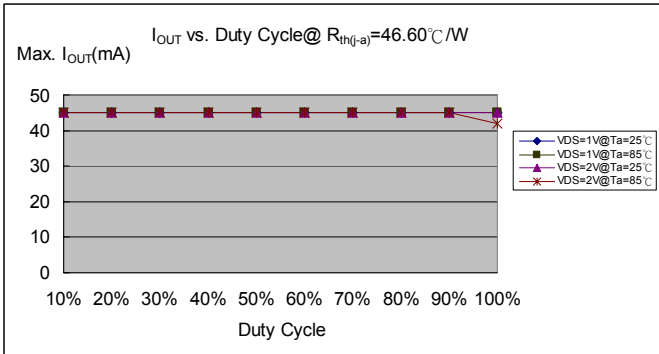


*Note1: For details, please refer to Macroblock’s “Policy on Pb-free & Green Package”.

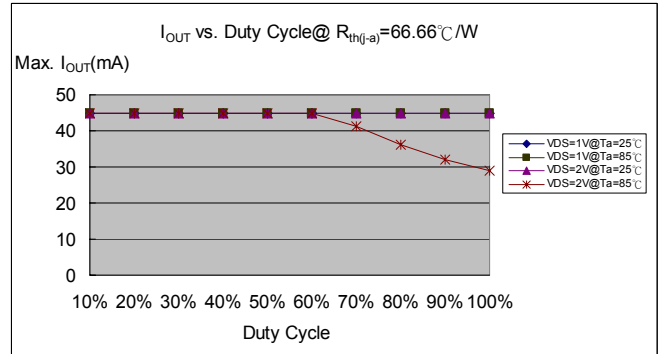
Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max) = (T_j - T_a) / R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act) = (I_{DD} \times V_{DD}) + (I_{OUT} \times Duty \times V_{DS} \times 16)$. Therefore, to keep $P_D(act) \leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

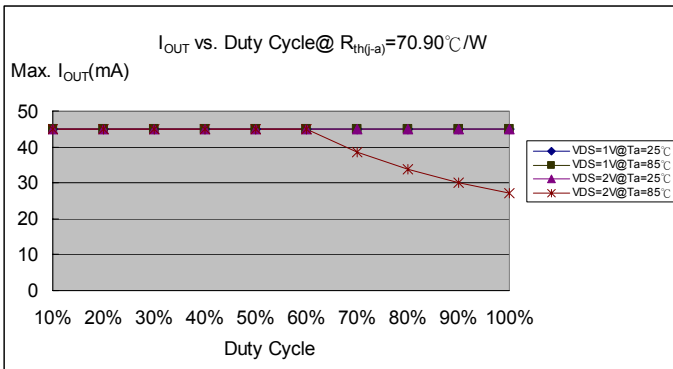
$$I_{OUT} = \{ [(T_j - T_a) / R_{th(j-a)}] - (I_{DD} \times V_{DD}) \} / V_{DS} / Duty / 16, \text{ where } T_j = 150^\circ\text{C}.$$



MBI5025GD



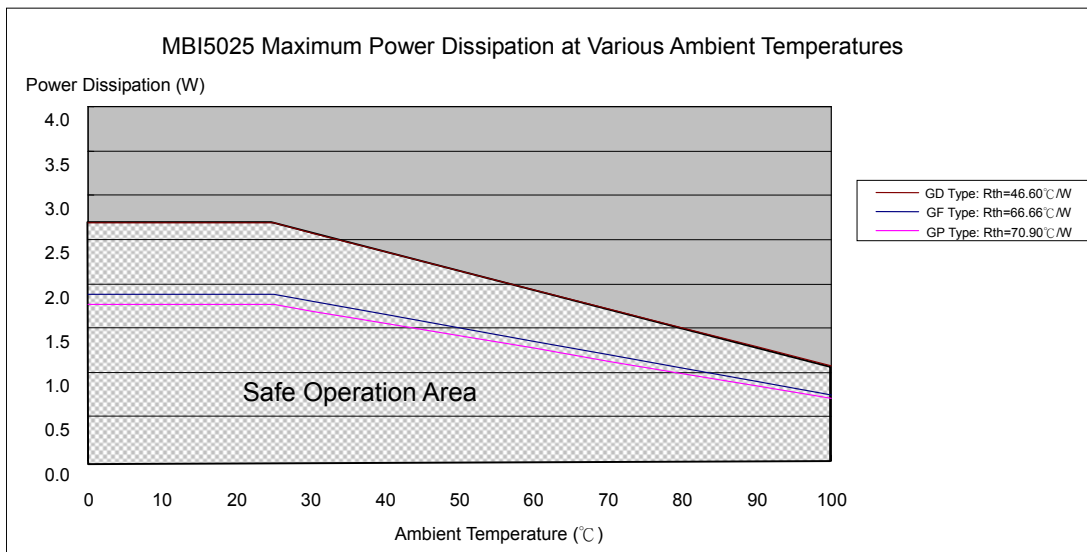
MBI5025GF



MBI5025GP

| Condition: $I_{OUT} = 45\text{mA}$, 16 output Channels | |
|---|---|
| Device Type | $R_{th(j-a)}$ ($^\circ\text{C}/\text{W}$) |
| GD | 46.60 |
| GF | 66.66 |
| GP | 70.90 |

The maximum power dissipation, $P_D(max) = (T_j - T_a) / R_{th(j-a)}$, decreases as the ambient temperature increases.

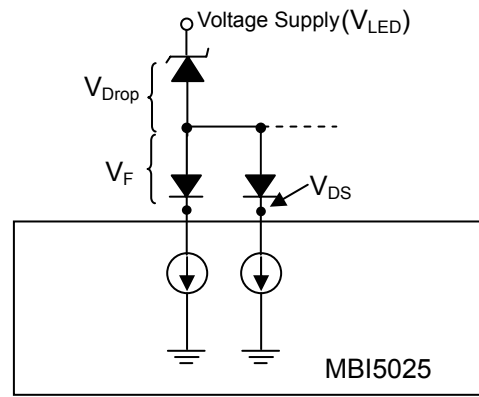
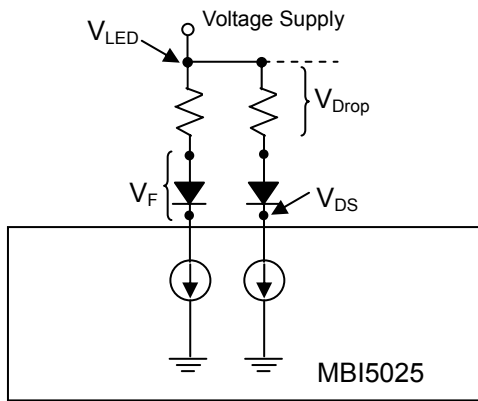


Load Supply Voltage (V_{LED})

MBI5025 are designed to operate with V_{DS} ranging from 0.4V to 0.8V (depending on $I_{OUT}=3\sim 45mA$) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)} > P_{D(max)}$ when $V_{LED} = 5V$ and $V_{DS} = V_{LED} - V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP} .

A voltage reducer lets $V_{DS} = (V_{LED} - V_F) - V_{DROP}$.

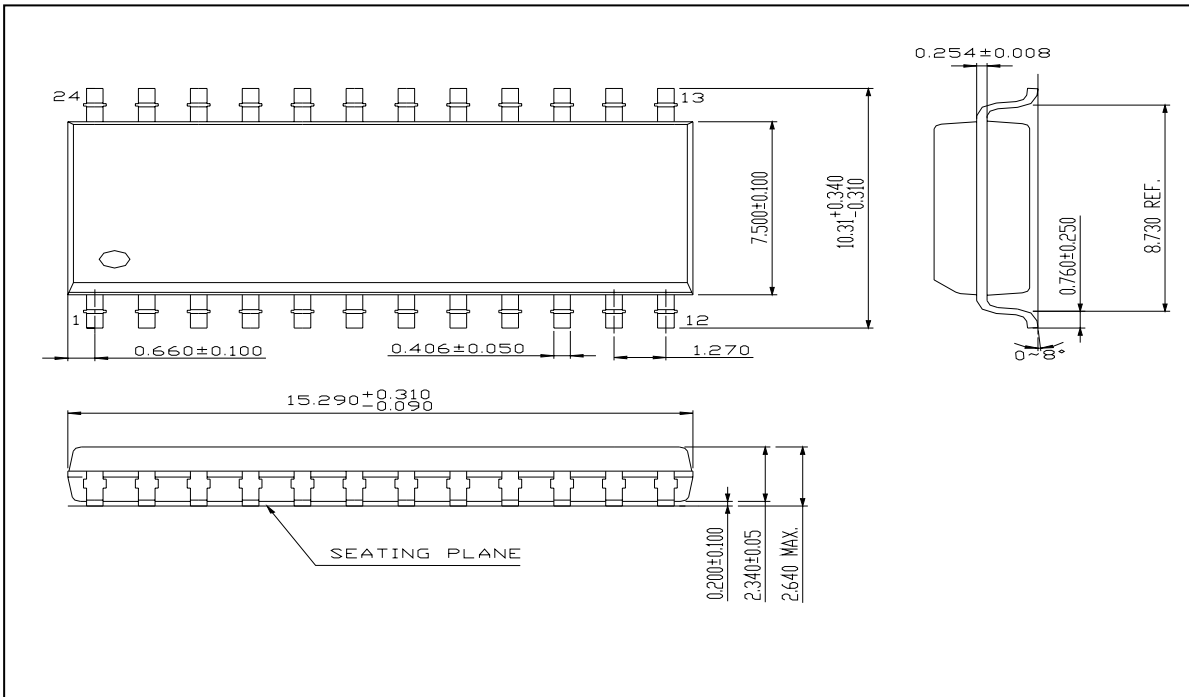
Resistors or Zener diode can be used in the applications as shown in the following figures.



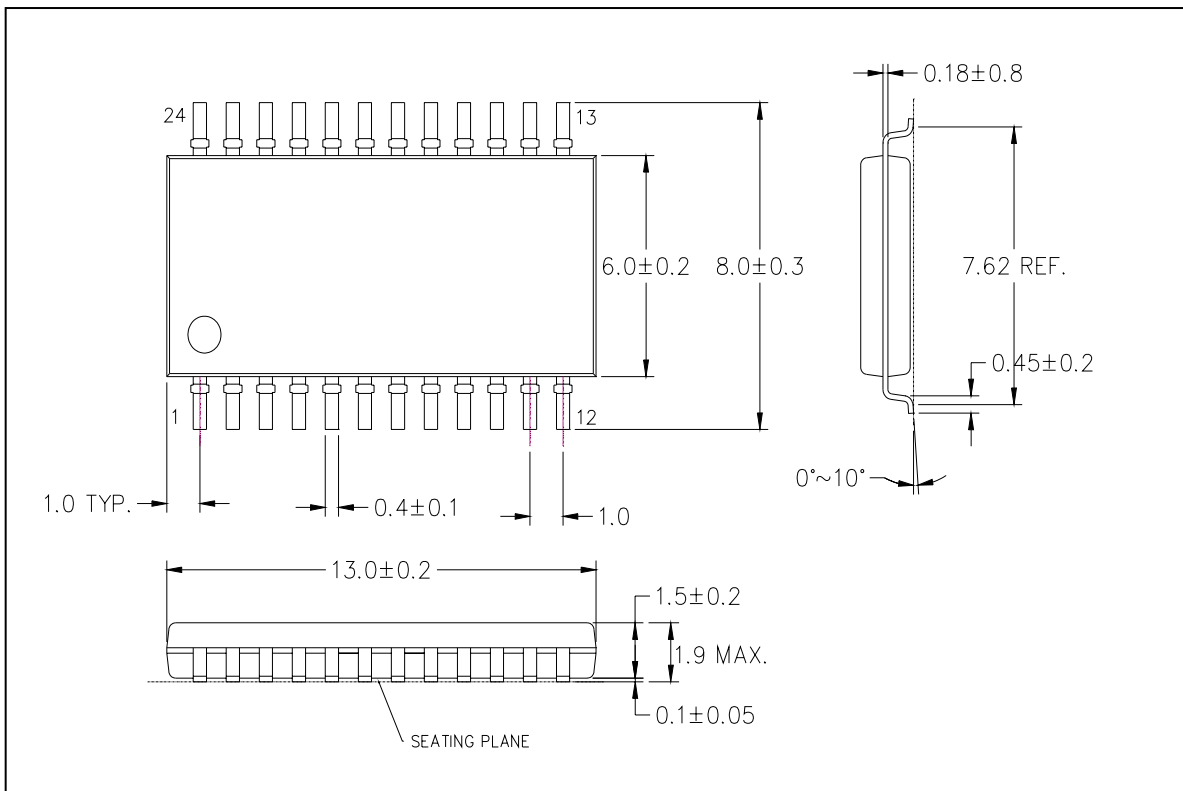
Switching Noise Reduction

LED driver ICs are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

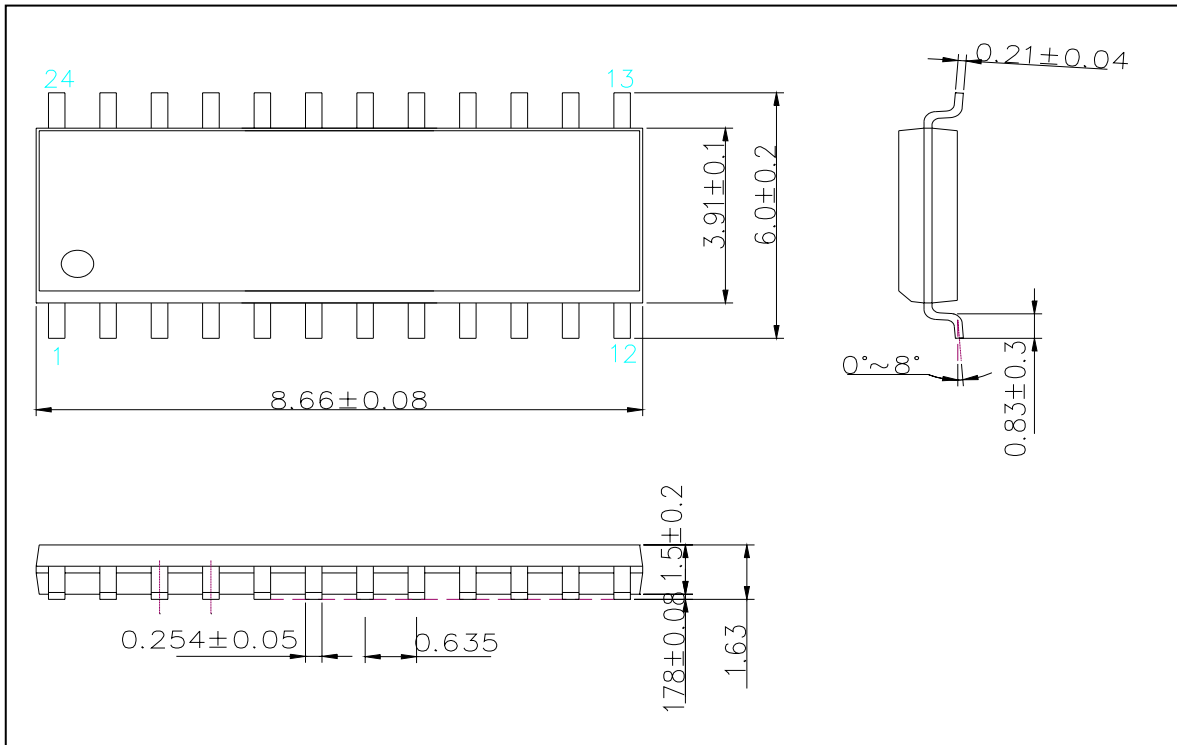
Package Outline



MBI5025GD Outline Drawing

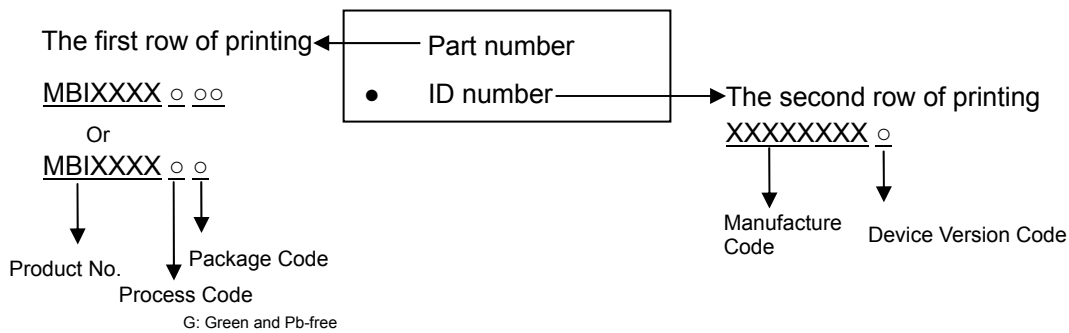


MBI5025GF Outline Drawing



MBI5025GP Outline Drawing

Product Top-mark Information



Product Revision History

| Datasheet version | Device version code |
|-------------------|---------------------|
| V1.00 | A |
| VA.00 | A |

Product Ordering Information

| Part Number | “Pb-free & Green” Package Type | Weight (g) |
|-------------|-----------------------------------|------------|
| MBI5025GD | SOP24-300-1.27 | 0.617 |
| MBI5025GF | SOP24-300-1.00 | 0.28 |
| MBI5025GP | SSOP24-150-0.64 | 0.11 |

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